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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/767,065	01/29/2004	Toshiharu Furukawa	ROC920030268US1	5663

30206 7590 02/01/2007

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EXAMINER	
NADAV, ORI	
ART UNIT	**PAPER NUMBER**
2811	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/01/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/767,065	FURUKAWA ET AL.	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-10 and 25-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-10 and 25-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

In view of the appeal brief filed on 10/27/2006, PROSECUTION IS HEREBY REOPENED. A new rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 25-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakamoto (6,097,138).

Nakamoto teaches in figure 16 and related text a semiconductor device structure, comprising:

a substrate 112;

an electrically conductive first plate 116 disposed on said substrate,

an electrically conductive second plate 176 disposed vertically above said first plate;

an electrically conductive layer 128 disposed between said first and second plates;

at least one nanotube 122 having an end electrically coupled with said first plate for increasing an effective area of said first plate, said at least one nanotube positioned in said electrically conductive layer; and

a dielectric layer 173 coating said length of said at least one nanotube such that said at least one nunotube is electrically isolated from said electrically conductive layer and said second plate,

wherein said at least one nanotube has a conducting molecular structure,

wherein said at least one nanotube has a semiconducting molecular structure, and

wherein said dielectric layer defines a coating that encases said at least one nanotube.

Claims 1, 4-6, 8 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Farnworth et al. (6,858,891).

Regarding claim 1, Farnworth et al. teach in figure 1 and related text a vertical semiconductor device structure, comprising:

a substrate 12 defining a substantially horizontal plane;

a source region 17;

a drain region 21;

a gate electrode 19 disposed on said substrate and being electrically insulated therefrom, said gate electrode positioned vertically between said source and drain regions; and

at least one semiconducting nanotube 22 including a first end electrically coupled with said source region, a second end electrically coupled with said drain region, and a channel region extending vertically through said gate electrode between said source and drain regions, said channel region being electrically insulated from said gate electrode, and

said gate electrode configured to receive a control voltage effective to regulate current flow through said channel region of said at least one semiconducting nanotube between said source region and said drain region (column 3, lines 55-56 and column 7, lines 41-42).

Regarding claims 4-6, 8 and 10, Farnworth et al. teach in figure 1 and related text an insulating layer disposed between said drain and said gate electrode for electrically

isolating said drain from said gate electrode, an insulating layer disposed between said source and said gate electrode for electrically isolating said source from said gate electrode, wherein said at least one semiconducting nanotube is composed of arranged carbon atoms, wherein said at least one semiconducting nanotube defines a channel region of a field effect transistor having a channel along which current flow is regulated by application of a control voltage to said gate electrode, wherein said at least one semiconducting nanotube is oriented substantially perpendicular to said horizontal plane, and wherein said gate dielectric is disposed on said at least one semiconducting nanotube.

Claims 1, 4-6, 8 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Choi et al. (6,566,704).

Regarding claim 1, Choi et al. teach in figure 3F and related text a vertical semiconductor device structure, comprising:

a substrate 200 defining a substantially horizontal plane;

a source region 40;

a drain region 50;

a gate electrode 20 disposed on said substrate and being electrically insulated therefrom, said gate electrode positioned vertically between said source and drain regions; and

at least one semiconducting nanotube 100 including a first end electrically coupled with said source region, a second end electrically coupled with said drain region, and a channel region extending vertically through said gate electrode between said source and drain regions, said channel region being electrically insulated from said gate electrode, and

said gate electrode configured to receive a control voltage effective to regulate current flow through said channel region of said at least one semiconducting nanotube between said source region and said drain region.

Regarding claims 4-6, 8 and 10, Choi et al. teach in figure 1 and related text an insulating layer 30 disposed between said drain and said gate electrode for electrically isolating said drain from said gate electrode, an insulating layer 10 disposed between said source and said gate electrode for electrically isolating said source from said gate electrode, wherein said at least one semiconducting nanotube is composed of arranged carbon atoms, wherein said at least one semiconducting nanotube defines a channel region of a field effect transistor having a channel along which current flow is regulated by application of a control voltage to said gate electrode, wherein said at least one semiconducting nanotube is oriented substantially perpendicular to said horizontal plane, and wherein said gate dielectric is disposed on said at least one semiconducting nanotube.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-3 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farnworth et al. (6,858,891).

Regarding claim 9, Farnworth et al. teach in figure 1 substantially the entire claimed structure, as applied to claim 1 above, except a plurality of semiconducting nanotubes extending vertically through said gate electrode. Farnworth et al. teach in figure 2 a plurality of semiconducting nanotubes 22 extending vertically through said gate electrode. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a plurality of semiconducting nanotubes extending vertically through said gate electrode in Farnworth et al.'s device in order to use the device in an practical application which requires plurality of nanotubes.

Regarding claims 2-3, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the source and drain of a catalyst material effective for growing said at least one semiconducting nanotube in Farnworth et al.'s device in order to simplify the processing steps of making the device.

Note that the process limitations of forming the source and drain of a catalyst material effective for growing said at least one semiconducting nanotube, would not carry

patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Claims 2-3 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi et al.

Regarding claim 9, Choi et al. teach in figure 3F substantially the entire claimed structure, as applied to claim 1 above, except a plurality of semiconducting nanotubes extending vertically through said gate electrode. Choi et al. teach in figure 4B a plurality of semiconducting nanotubes 100. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a plurality of semiconducting nanotubes extending vertically through said gate electrode in Choi et al.'s device in order to use the device in an practical application which requires plurality of nanotubes.

Regarding claims 2-3, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the source and drain of a catalyst material effective for growing said at least one semiconducting nanotube in Choi et al.'s device in order to simplify the processing steps of making the device.

Note that the process limitations of forming the source and drain of a catalyst material effective for growing said at least one semiconducting nanotube, would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Claims 25-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamoto (6,097,138) in view of Jin et al. (6,250,984).

Nakamoto teaches in figure 16 and related text a semiconductor device structure, comprising:

a substrate 112;

an electrically conductive first plate 116 disposed on said substrate,

an electrically conductive second plate 176 disposed vertically above said first plate;

an electrically conductive layer 128 disposed between said first and second plates;

at least one nanotube 122 having an end electrically coupled with said first plate for increasing an effective area of said first plate, said at least one nanotube positioned in said electrically conductive layer; and

a dielectric 173 coating said length of said at least one nanotube such that said at least one nunotube is electrically isolated from said electrically conductive layer and said second plate,

wherein said at least one nanotube has a conducting molecular structure,

wherein said at least one nanotube has a semiconducting molecular structure, and

wherein said dielectric defines a coating that encases said at least one nanotube.

Nakamoto does not explicitly state that dielectric 173 is a layer.

Jin et al. teach in figure 11 and related text a dielectric 101A coating said length of said at least one nanotube.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a dielectric layer in Nakamoto's device in order to provide better protection to the nanotubes.

Response to Arguments

Applicant's arguments with respect to claims 1-6, 8-10 and 25-28 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
1/30/07

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